WHAT IS CLAIMED IS:

1. A current compensation circuit for use with a current mirror circuit, the current mirror circuit having a current path defined by a first programmable current mirror stage driving a first fanout current mirror stage, the first programmable current mirror stage having at least one transistor with a channel length exhibiting a first channel length modulation factor λ_1, the first fanout current mirror stage coupled to a supply voltage source, the current compensation circuit comprising:

a supply voltage current mirror coupled to the supply voltage source, and having a current output coupled to the current path; and

a second programmable current mirror coupled in series with the supply voltage current mirror and having at least one transistor with a channel length exhibiting a channel length modulation factor λ_2, wherein the second channel length modulation factor λ_2 is larger than the first channel length modulation factor λ_1, the first programmable current mirror and the second programmable current mirror cooperating to maintain a bias current through the first fanout current mirror stage substantially independent of changes in the supply voltage.

2. A current compensation circuit according to claim 1 wherein each of the programmable current mirror stages comprises:

a parallel array of programmable transistors for defining a predetermined range of current.

3. A current compensation circuit according to claim 1 wherein the current compensation circuit is formed on a single integrated circuit device.

4. A current compensation circuit according to claim 3 wherein the current compensation circuit is formed in CMOS.

5. A current compensation circuit for use with a current mirror circuit, the current mirror circuit having a current path defined by a first programmable current mirror stage driving a first fanout current mirror stage, the first programmable current mirror stage having at least one transistor with a channel length exhibiting a first channel length modulation factor λ_1, the first fanout current mirror stage coupled to a supply voltage source, the current compensation circuit comprising:

means for detecting changes in the supply voltage from the supply voltage source, the means for detecting changes including means for generating a compensation signal representative of voltage changes in the supply voltage source; and

means for generating a compensation current for application to the current mirror in response to the compensation signal.

6. A current compensation circuit according to claim 5 wherein the means for detecting changes in the supply voltage comprises:

a supply voltage current mirror coupled to the supply voltage source, and having a current output coupled to the current path; and

a second programmable current mirror coupled in series with the supply voltage current mirror.

7. A current compensation circuit according to claim 6 wherein:

the second programmable current mirror includes at least one transistor with a channel length exhibiting a channel length modulation factor λ_2, such that the second channel length modulation factor λ_2 is larger than the first channel length modulation factor λ_1; and

the means for generating a compensation current comprises the first and second programmable current mirrors cooperating to maintain a bias current through the first fanout current mirror stage substantially independent of changes in the supply voltage.

8. A method for compensating for supply-voltage-induced changes to a desired current through a fanout current mirror, the method including the steps:

detecting changes in the supply voltage from a supply voltage source;

generating a compensation current to a current path node, the compensation current representative of the voltage changes in the supply voltage source, the compensation current based on the channel length modulation factor $\lambda 2$ of a second programmable current source; and

sinking current from the current path node with a first programmable current source having a first channel length modulation factor $\lambda 1$ less than that of $\lambda 2$, wherein the level of current sunk corresponds to the difference between the compensation current and the desired current through the fanout current mirror.

9. A timing generator for use in a semiconductor tester, the timing generator including:

a delay line having a plurality of delay cells with respective phase-shifted outputs and bias current inputs;

a selector having a plurality of inputs for receiving the phase shifted outputs, and an output;

phase detection circuitry for detecting the phase shift between the selector output and a reference signal, and generating bias current; and

fanout circuitry to distribute the bias current to the plurality of delay cells, the fanout circuitry comprising a first programmable current mirror circuit and a first fanout current mirror circuit coupled to a supply voltage, the first programmable current mirror circuit and the fanout current mirror circuit cooperating to define a bias current path, and

a current compensation circuit coupled to the fanout circuitry to minimize changes to the bias current resulting from changes in the supply voltage, the current compensation circuit including at least two programmable current mirrors, each having respective channel length modulation factors $\lambda 1$ and $\lambda 2$, one of the channel length modulation factors being larger than the other.

10. A timing generator according to claim 9 wherein the first programmable current mirror stage having at least one transistor with a channel length exhibiting a first channel length modulation factor λ_1, the current compensation circuit comprising:

a supply voltage current mirror coupled to the supply voltage source, and having a current output coupled to the current path; and

a second programmable current mirror coupled in series with the supply voltage current mirror and having at least one transistor with a channel length exhibiting a channel length modulation factor λ_2, wherein the second channel length modulation factor λ_2 is larger than the first channel length modulation factor λ_1, the first programmable current mirror and the second programmable current mirror cooperating to maintain a bias current through the first fanout current mirror stage substantially independent of changes in the supply voltage.

11. A timing generator for use in a semiconductor tester, the timing generator including:

a delay line having a plurality of delay cells with respective phase-shifted outputs and bias current inputs;

a selector having a plurality of inputs for receiving the phase shifted outputs, and an output;

phase detection circuitry for detecting the phase shift between the selector output and a reference signal, and generating bias current; and

means for distributing the bias current to the plurality of delay cells.

12. A timing generator according to claim 11 wherein the means for distributing comprises:

fanout circuitry to distribute the bias current to the plurality of delay cells, the fanout circuitry comprising

a first programmable current mirror circuit, the first programmable current mirror circuit having at least one transistor exhibiting a channel length modulation factor $\lambda 1$;

a fanout current mirror circuit coupled to a supply voltage, the fanout current mirror and the first programmable current mirror circuits coupled at a current node and cooperating to define a bias current path, and

a current compensation circuit comprising

a supply voltage current mirror coupled to the supply voltage source, and having a current output coupled to the current path; and

a second programmable current mirror coupled in series with the supply voltage current mirror and having at least one transistor with a channel length exhibiting a channel length modulation factor $\lambda 2$, wherein the second channel length modulation factor $\lambda 2$ is larger than the first channel length modulation factor $\lambda 1$, the first programmable current mirror and the second programmable current mirror cooperating to maintain a bias current through the first fanout current mirror stage substantially independent of changes in the supply voltage.